Claims

What is claimed is:

1. A method of forming an electrical structure, comprising:

forming a complex power-signal (CPS) substructure;

testing an electrical performance of the CPS substructure to determine whether the CPS substructure satisfies electrical performance acceptance requirements, wherein the testing includes testing for at least one of electrical integrity and electrical signal delay, and wherein the testing for electrical integrity includes testing for at least one of an electrical short, an electrical open, and an erroneous impedance; and

if the testing determines that the CPS substructure satisfies the electrical performance acceptance requirements, then forming a dielectric-metallic (DM) laminate on a first external surface of the CPS substructure including forming a first multilevel conductive via through the DM laminate, wherein the DM laminate includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on the first external surface of the CPS substructure, wherein N is at least 2, and wherein the multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

2. The method of claim 1, further comprising following the testing: if the testing determines that the CPS substructure does not satisfy the electrical performance acceptance requirements, then forming a new CPS substructure that replaces and thus becomes the CPS substructure and

repeating testing an electrical performance of the CPS substructure so replaced.

3. The method of claim 1, wherein the first multilevel conductive via is a stacked via.

4. The method of claim 1, wherein the first multilevel conductive via is a deep via.

5. The method of claim 1, wherein the first multilevel conductive via is a simple-deep via

6. The method of claim 1, wherein the first multilevel conductive via is a stacked-deep via.

7. The method of claim 1, wherein the CPS substructure is a single CPS substructure.

8. The method of claim 1, wherein the CPS substructure is a double CPS substructure.

9. The method of claim 1, wherein N=2.

10. The method of claim 1, further comprising forming a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

11. The method of claim 1, wherein the first metal layer is at the first external surface of the CPS substructure.

12. The method of claim 1, further comprising forming a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

13. The method of claim 12, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

14. The method of claim 12, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

15. The method of claim 12, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein first metal layer is at the second external surface.

16. The method of claim 1, further comprising coupling a semiconductor chip to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

17. A method of forming an electrical structure, comprising:

forming a complex power-signal (CPS) substructure;

testing an electrical performance of the CPS substructure to determine whether the CPS substructure satisfies first electrical performance acceptance requirements, wherein the testing includes testing for at least one of electrical integrity and electrical signal delay, and wherein the testing for electrical integrity includes testing for at least one of an electrical short, an electrical open, and an erroneous impedance; and

if the testing determines that the CPS substructure satisfies the first electrical performance acceptance requirements, then forming a dielectric-metallic (DM) laminate on a first external surface of the CPS substructure including forming a first multilevel conductive via through the DM laminate,

wherein the DM laminate includes an alternating sequence an equal number of dielectric layers and metallic layers such that a first dielectric layer of the dielectric layers is formed on the first external surface of the CPS substructure,

wherein the multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure,

wherein after each metallic layer of the metallic layers is formed, examining an electrical performance of the electrical structure formed thus far to determine whether the electrical structure satisfies second electrical performance acceptance requirements,

wherein the examining includes examining for at least one of an electrical integrity and electrical signal delay,

wherein the examining for electrical integrity includes examining for at least one

of an electrical short, an electrical open, and an erroneous impedance, and

wherein if the examining determines that the electrical structure satisfies the second electrical performance acceptance requirements, then continuing forming the DM laminate if less than N metallic layers have been formed else ending forming the DM laminate, and

wherein N is at least 2.

18 . The method of claim 17, further comprising following the testing: if the testing determines that the CPS substructure does not satisfy the first electrical performance acceptance requirements, then forming a new CPS substructure that replaces and thus becomes the CPS substructure and repeating testing an electrical performance of the CPS substructure so replaced.

19 . The method of claim 17, further comprising following the examining: if the examining determines that the electrical structure does not satisfy the second electrical performance acceptance requirements, then discontinuing forming the DM laminate.

20. A method of forming an electrical structure, comprising:

forming a complex power-signal (CPS) substructure;

testing an electrical performance of the CPS substructure to determine whether the CPS substructure satisfies electrical performance acceptance requirements, wherein the testing includes testing for at least one of an electrical integrity and electrical signal delay, and wherein the testing for electrical integrity includes testing for at least one of an electrical short, an electrical open, and an erroneous impedance; and

if the testing determines that the CPS substructure satisfies the electrical performance acceptance requirements then:

forming a first dielectric-metallic (DM) laminate on a first external surface of the CPS substructure including forming a first multilevel conductive via through the first DM laminate, wherein the first DM laminate includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on the first external surface of the CPS substructure, wherein N is at least 2, and wherein the multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure, and

forming a second DM laminate on a second external surface of the CPS substructure including forming a second multilevel conductive via through the second DM laminate, wherein the second DM laminate includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on the second external surface of the CPS substructure, wherein M is at least 2, and wherein the multilevel conductive via is electrically coupled

to a second metal layer of the CPS substructure.

21. The method of claim 20, wherein M=N.

22. The method of claim 20, wherein forming the first DM laminate and forming the second DM laminate comprise forming the first and second DM laminates symmetrically with respect to the CPS substructure.

23. The method of claim 20, further comprising forming a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the CPS substructure, and the second DM laminate.

24. A method of forming an electrical structure, comprising:

forming a first complex power-signal (CPS) substructure;

testing an electrical performance of the first CPS substructure to determine whether the first CPS substructure satisfies electrical performance acceptance requirements, wherein the testing includes testing for at least one of an electrical integrity and electrical signal delay, and wherein the testing for electrical integrity includes testing for at least one of an electrical short, an electrical open, and an erroneous impedance;

forming a second complex power-signal (CPS) substructure;

examining an electrical performance of the second CPS substructure to determine whether the second CPS substructure satisfies the electrical performance acceptance requirements, wherein the examining includes examining for at least one of an electrical integrity and electrical signal delay, and wherein the examining for electrical integrity includes examining for at least one of an electrical short, an electrical open, and an erroneous impedance;

if the testing determines that the first CPS substructure satisfies the electrical performance acceptance requirements and if the examining determines that the second CPS substructure satisfies the electrical performance acceptance requirements, then:

forming a composite CPS substructure by coupling a first surface of the first CPS substructure to a first surface of an interfacing dielectric layer and coupling a first surface of the second CPS substructure to a second surface of the interfacing dielectric layer;

forming a first dielectric-metallic (DM) laminate on a second surface of the first CPS substructure including forming a first multilevel conductive via through the first DM laminate, wherein the first DM laminate includes an alternating sequence of an equal

number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on the second surface of the first CPS substructure, wherein N is at least 2, and wherein the first multilevel conductive via is electrically coupled to a metal layer of the first CPS substructure, and

forming a second DM laminate on a second surface of the second CPS substructure including forming a second multilevel conductive via through the second DM laminate, wherein the second DM laminate includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on the second surface of the second CPS substructure, wherein M is at least 2, and wherein the second multilevel conductive via is electrically coupled to a metal layer of the second CPS substructure.

25. The method of claim 24, wherein M=N.

26. The method of claim 24, wherein forming the first DM laminate and forming the second DM laminate comprise forming the first and second DM laminates symmetrically with respect to the composite CPS substructure.

27. The method of claim 24, further comprising forming a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the composite CPS substructure, and the second DM laminate.

28. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2; and

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

29. The electrical structure of claim 28, wherein the first multilevel conductive via is a stacked via.

30. The electrical structure of claim 28, wherein the first multilevel conductive via is a deep via.

31. The electrical structure of claim 28, wherein the first multilevel conductive via is a simple-deep via

32. The electrical structure of claim 28, wherein the first multilevel conductive via is a stacked-deep via.

33. The electrical structure of claim 28, wherein the CPS substructure is a single CPS substructure.

34. The electrical structure of claim 28, wherein the CPS substructure is a double CPS substructure.

35. The electrical structure of claim 28, wherein N=2.

36. The electrical structure of claim 28, further comprising a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

37. The electrical structure of claim 28, wherein the first metal layer is at the first external surface of the CPS substructure.

38. The electrical structure of claim 28, further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

39. The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

40. The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

41. The electrical structure of claim 38, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein first metal layer is at the second external surface.

42. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has satisfied an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure; and

a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure.

43. The electrical structure of claim 42, wherein M=N.

44. The electrical structure of claim 42, further comprising a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the CPS substructure, and the second DM laminate.

45. An electrical structure, comprising:

a composite complex power-signal (CPS) substructure that includes an interfacing dielectric layer sandwiched between a first CPS substructure and a second CPS substructure, wherein a first surface of the first CPS substructure is coupled to a first surface of the interfacing dielectric layer, and wherein a first surface of the second CPS substructure is coupled to a second surface of the interfacing dielectric layer,

said first CPS substructure having passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance, and

said second CPS substructure having passed the electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance,

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a second surface of the first CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a metal layer of the first CPS substructure; and

a second DM laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second surface of the second CPS substructure, wherein M is at least 2, and wherein

a second multilevel conductive via through the second DM laminate is electrically coupled to a metal layer of the second CPS substructure.

46. The electrical structure of claim 45, wherein M=N.

47. The electrical structure of claim 45, further a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the composite CPS substructure, and the second DM laminate.

48. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2;

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

49. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and erroneous an impedance;

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure;

a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

50. An electrical structure, comprising:

a composite complex power-signal (CPS) substructure that includes an interfacing dielectric layer sandwiched between a first CPS substructure and a second CPS substructure, wherein a first surface of the first CPS substructure is coupled to a first surface of the interfacing dielectric layer, and wherein a first surface of the second CPS substructure is coupled to a second surface of the interfacing dielectric layer,

said first CPS substructure having passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, electrical open, and erroneous impedance, and

said second CPS substructure having passed the electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance,

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a second surface of the first CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a metal layer of the first CPS substructure;

a second DM laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second surface of the second CPS substructure, wherein M is at least 2, and wherein

a second multilevel conductive via through the second DM laminate is electrically coupled to a metal layer of the second CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the first CPS substructure.

51. An electrical structure, comprising:

a complex power-signal (CPS) substructure;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2; and

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

52. The electrical structure of claim 51, wherein the first multilevel conductive via is a stacked via.

53. The electrical structure of claim 51, wherein the first multilevel conductive via is a deep via.

54. The electrical structure of claim 51, wherein the first multilevel conductive via is a simple-deep via

55. The electrical structure of claim 51, wherein the first multilevel conductive via is a stacked-deep via.

56. The electrical structure of claim 51, wherein the CPS substructure is a single CPS substructure.

57. The electrical structure of claim 51, wherein the CPS substructure is a double CPS substructure.

58. The electrical structure of claim 51, wherein N=2.

59. The electrical structure of claim 51, further comprising a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

60. The electrical structure of claim 51, wherein the first metal layer is at the first external surface of the CPS substructure.

61. The electrical structure of claim 51, further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

62. The electrical structure of claim 51, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

63. The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

64. The electrical structure of claim 38, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein first metal layer is at the second external surface.

65. The method of claim 38, further comprising a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.